CLAIMS

1. A method for displaying frames, said method comprising:

displaying a first portion of a frame; and

writing a second portion of the frame while displaying the first portion of the frame.

2. The method of claim 1, wherein writing the second portion of the frame further comprises:

overwriting a third portion of the frame with the second portion of the frame.

3. The method of claim 1, wherein writing the second portion of the frame further comprises:

decoding the second portion of the frame.

4. The method of claim 1, further comprising:

displaying the second portion of the frame responsive to displaying the first portion of the frame;

overwriting the first portion of the frame with a fourth portion of the frame.

5. The method of claim 1, further comprising:

displaying the second portion of the frame responsive to displaying the first portion of the frame; and

overwriting the first portion of the frame with a first portion of another frame while displaying the second portion of the frame.

6. The method of claim 1, wherein the frame comprises a high definition television frame.

7. A circuit for displaying frames, said circuit comprising:

a memory for storing a first portion of a frame;

a display engine for displaying the first portion of the frame; and

a controller for writing a second portion of the frame in the memory, while the display engine displays the first portion.

8. The circuit of claim 7, wherein the controller overwrites a third portion of the frame with the second portion of the frame in the memory.

9. The circuit of claim 7, wherein the controller decodes the second portion of the frame.

10. The circuit of claim 7, wherein:

the display engine displays the second portion of the frame responsive to displaying the first portion of the frame; and

the controller overwrites the first portion of the frame with a fourth portion of the frame in the memory.

11. The circuit of claim 7, wherein:

the display engine displays the second portion of the frame responsive to displaying the first portion of the frame; and

the controller overwrites the first portion of the frame with a first portion of another frame while the display engine displays the second portion of the frame.

12. The circuit of claim 7, wherein the memory further comprises:

a first prediction frame buffer for storing a first prediction frame;

a second prediction frame buffer for storing a second prediction frame; and

a delta frame buffer for storing the first portion of the frame and the second portion of the frame.

13. The circuit of claim 13, wherein the memory comprises no more than 4 megabytes, and wherein the frame and the first prediction frame and the second prediction frame comprise high definition television frames with at least 1280x720 resolution.

14. The circuit of claim 13, wherein the memory comprises no more than 8 megabytes, and wherein the frame and the first prediction frame and the second prediction frame comprise high definition television frames with at least 1920x1080 resolution.

15. An integrated circuit for storing decoded frames, said integrate circuit comprising:

a first prediction frame buffer for storing a first frame;

a second prediction frame buffer for storing a second frame; and

a delta frame buffer for storing a portion of a third frame.

16. The integrated circuit of claim 15, wherein the integrated circuit comprises no more than 4 megabytes of memory, and wherein the first frame and the second frame and the third frame comprise high definition television frames with at least 1280x720 resolution.

17. The integrated circuit of claim 15, wherein the integrated circuit comprises no more than 8 megabytes of memory, and wherein the first frame and the second frame and the third frame comprise high definition television frames with at least 1920x1080 resolution.